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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,241	10/17/2001	Robbert Christiaan Van Ommering	PHNL 000550	7627

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,241	VAN OMMERING, ROBBERT CHRISTIAAN	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 2, 8, 10 and 11 are withdrawn in view of the newly discovered reference(s) to Shteyn (U.S. Patent 6,918,123). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over WOLD (U.S. Patent 5,386,568) in view of SHTEYN (U.S. Patent 6,918,123).

As to claim 1, WOLD teaches in an audio apparatus (music synthesizer) (col. 19, lines 57-61; col. 5, lines 26-31), a method of controlling an arrangement of a plurality of hardware components (hardware devices / hardware components) at least some of which are coupled to one another via signal leads (cables / wires), by means of a data processing unit (embedded processors) (col. 19, lines 28-31; col. 19, lines 42-46; col. 19, line 55 – col. 20, line 3) and a computer program (software) which is executed therein, characterized in that the computer program comprises a plurality of sub-modules (software modules) (col. 11, lines 2-5; col. 4, lines 65-67) which correspond (are associated) to the hardware components (hardware devices / hardware components) and are connected via data channels (via input / output communication

software connections) in conformity with the real signal leads (cables / wires) between the hardware components (hardware devices) (col. 11, lines 7-33; col. 12, lines 43-66; col. 19, lines 2-5; col. 19, lines 34-42; col. 9, lines 61-68; col. 20, lines 14-17; col. 19, lines 52-68; col. 24, lines 42-55). However, WOLD does not allude to communication occurs between the sub-modules to control the hardware components.

SHTEYN teaches a plurality of hardware components (physical components) represented by a plurality of sub-modules (software objects) wherein the invocations between the sub-modules control the communication of the hardware components (col. 4, lines 21-27; col. 7, lines 26-37; col. 8, lines 45-60). Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of WOLD with the teachings of SHTEYN in order to facilitate the software route linking of objects based on device configuration (col. 3, lines 1-12; col. 4, lines 19-27).

As to claim 2, WOLD teaches in an audio apparatus (music synthesizer) (col. 19, lines 57-61; col. 5, lines 26-31), a method of controlling an arrangement of a plurality of hardware components (hardware devices / hardware components) at least some of which are coupled to one another via signal leads (cables / wires), by means of a data processing unit (embedded processors) (col. 19, lines 28-31; col. 19, lines 42-46; col. 19, line 55 – col. 20, line 3) and a computer program (software) which is executed therein, characterized in that the computer program comprises a plurality of sub-modules (software modules) (col. 11, lines 2-5; col. 4, lines 65-67) which correspond (are associated) to the hardware components (hardware devices / hardware

components) and are connected via data channels (via input / output communication software connections) in conformity with the real signal leads (cables / wires) between the hardware components (hardware devices) (col. 11, lines 7-33; col. 12, lines 43-66; col. 19, lines 2-5; col. 19, lines 34-42; col. 9, lines 61-68; col. 20, lines 14-17; col. 19, lines 52-68; col. 24, lines 42-55). However, WOLD does not allude to the sub-modules or the data channels between the sub-modules are adapted in conformity with the dynamic changing of the hardware components and/ or the signal leads between the hardware components.

SHTEYN teaches a plurality of hardware components (physical components) represented by a plurality of sub-modules (software objects) wherein the invocations (routes) between the sub-modules are controlled by the changing of the hardware components or the signal leads between the hardware components (via the pluging in or unplugging of the modules / devices) (col. 4, lines 21-27; col. 7, lines 26-37; col. 8, lines 45-60). Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of WOLD with the teachings of SHTEYN in order to facilitate the software route linking of objects based on device configuration (col. 3, lines 1-12; col. 4, lines 19-27).

As to claim 3, WOLD teaches all data channels utilize the same communication protocol (col. 20, lines 17-19; col. 11, lines 2-25).

As to claim 4, WOLD teaches that the hardware components are printed circuit boards, layout cells, microchips and/or core cells (col. 19, lines 57-61).

As to claims 5 and 6, reference is made to an audio apparatus that corresponds to the method of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 7, WOLD teaches the sub-modules (software modules) have inputs and outputs (input / output objects) that correspond to input and outputs (input / output ports) for the hardware components (hardware modules) (col. 19, lines 61-64; col. 24, lines 42-52; col. 19, lines 28-46).

As to claim 8, WOLD teaches in an audio apparatus (music synthesizer) (col. 19, lines 57-61; col. 5, lines 26-31), a method of controlling an arrangement of a plurality of hardware components (hardware devices / hardware components) at least some of which are coupled to one another via signal leads (cables / wires), by means of a data processing unit (embedded processors) (col. 19, lines 28-31; col. 19, lines 42-46; col. 19, line 55 – col. 20, line 3) and a computer program (software) which is executed therein, characterized in that the computer program comprises a plurality of sub-modules (software modules) (col. 11, lines 2-5; col. 4, lines 65-67) which correspond (are associated) to the hardware components (hardware devices / hardware components) and are connected via data channels (via input / output communication software connections) in conformity with the real signal leads (cables / wires) between

the hardware components (hardware devices) (col. 11, lines 7-33; col. 12, lines 43-66; col. 19, lines 2-5; col. 19, lines 34-42; col. 9, lines 61-68; col. 20, lines 14-17; col. 19, lines 52-68; col. 24, lines 42-55). However, WOLD does not allude to a signals validity can be reported through the inputs and outputs to the sub-modules and the hardware components.

SHTEYN teaches a plurality of hardware components (physical components) represented by a plurality of sub-modules (software objects) wherein the invocations (routes) between the sub-modules are controlled by the changing of the hardware components or the signal leads between the hardware components (via the plugging in or unplugging of the modules / devices) (col. 4, lines 21-27; col. 7, lines 26-37; col. 8, lines 45-60). It would be obvious to one of ordinary skill in the art that the invocations contain multiple types of data, including indicators of the correctness of the message, i.e. its validity. Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of WOLD with the teachings of SHTEYN in order to facilitate the software route linking of objects based on device configuration (col. 3, lines 1-12; col. 4, lines 19-27).

As to claim 9, WOLD teaches hardware devices can establish connection through inputs and outputs (input object / output object / input port / output port) to the sub-modules (software modules) and the hardware components (hardware modules) (col. 19, lines 61-64; col. 24, lines 42-52; col. 19, lines 28-46). WOLD also states that the invention is not to be limited to a specific illustrated embodiment, but only to the

scope of the claims. However, neither WOLD nor SHTEYN teach that the hardware devices are switches. Official Notice is taken in that switches are well-known hardware devices and therefore would be obvious in view of the teachings of WOLD and SHTEYN in order to facilitate the communication between switches by using software modules and hardware components.

As to claims 10 and 11, WOLD teaches in an audio apparatus (music synthesizer) (col. 19, lines 57-61; col. 5, lines 26-31), a method of controlling an arrangement of a plurality of hardware components (hardware devices / hardware components) at least some of which are coupled to one another via signal leads (cables / wires), by means of a data processing unit (embedded processors) (col. 19, lines 28-31; col. 19, lines 42-46; col. 19, line 55 – col. 20, line 3) and a computer program (software) which is executed therein, characterized in that the computer program comprises a plurality of sub-modules (software modules) (col. 11, lines 2-5; col. 4, lines 65-67) which correspond (are associated) to the hardware components (hardware devices / hardware components) and are connected via data channels (via input / output communication software connections) in conformity with the real signal leads (cables / wires) between the hardware components (hardware devices) (col. 11, lines 7-33; col. 12, lines 43-66; col. 19, lines 2-5; col. 19, lines 34-42; col. 9, lines 61-68; col. 20, lines 14-17; col. 19, lines 52-68; col. 24, lines 42-55). However, WOLD does not allude to a signals properties can be defined through the inputs and outputs to the sub-modules and the hardware components.

SHTEYN teaches a plurality of hardware components (physical components) represented by a plurality of sub-modules (software objects) wherein the invocations (routes) between the sub-modules are controlled by the changing of the hardware components or the signal leads between the hardware components (via the plugging in or unplugging of the modules / devices) (col. 4, lines 21-27; col. 7, lines 26-37; col. 8, lines 45-60). SHTEYN teaches enabling or disabling of routes. Official Notice is taken in that It would be well known and obvious to one of ordinary skill in the art that the establishing of routes would entail passing connection properties and therefore, obvious in view of the teaching combination of WOLD and SHYTEYN that the enabling of the route would pass signal properties. Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of WOLD with the teachings of SHTEYN in order to facilitate the software route linking of objects based on device configuration (col. 3, lines 1-12; col. 4, lines 19-27).

As to claim 17, SHTEYN teaches the at least one of the hardware components is a tuner (col. 6, lines 19-41; col. 6, lines 48 – col. 7, line 11; col. 9, lines 11-18; col. 9, lines 47-53).

As to claim 18, SHTEYN teaches the at least one other of the hardware components is an output device operatively coupled to the tuner (col. 6, lines 19-41; col. 6, lines 48 – col. 7, line 11; col. 9, lines 11-18; col. 9, lines 47-53).

As to claim 19, SHTEYN teaches communications occur between the sub-modules to prevent output of the output device for a period of time (via enabling / disabling communication) (col. 4, lines 19-27).

As to claim 20, SHTEYN teaches there is at least another tuner operatively connected to the output device through a switching device (havi network) (col. 6, lines 19-41; col. 6, lines 48 – col. 7, line 11; col. 9, lines 11-18; col. 9, lines 47-53) and wherein communications occur between the sub-modules to prevent output of the output device for a period of time via the switching device (via enabling / disabling communication) (col. 7, lines 19-27).

As to claim 12, refer to claim 17 for rejection.

As to claim 13, refer to claim 18 for rejection.

As to claim 14, refer to claim 19 for rejection.

As to claim 15, refer to claim 20 for rejection.

As to claim 16, refer to claim 20 for rejection.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-7, 9 and 12-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

January 6, 2006